REMARKS

Reconsideration and further examination of this application is respectfully requested. Claims 1-6 have been further amended to clarify that the single multi-bit shift register is used for both data and instructions. Support for this clarification may be found throughout the original specification, and specifically in the first full paragraph on page 4 at lines 13-25. Claims 1-6 have also been amended to employ a single style of claim writing and to address a 35 U.S.C. 112 second paragraph problem with a list of potential, but indefinite, operations for the multi-core/dual expander. Applicants have removed the list of potential operations from claims 1-6. Applicants have added new claims 7-12 to include the list of potential operations as Markush group dependent claims for each of independent claims 1-6. Applicants have also added new dependent claims 13-18 depending from independent claims 1-6, respectively to add a limitation that EPROM does not need to be removed and reprogrammed. Support for new dependent claims 13-18 may be found on page 9 at lines 26-18 of the original specification. There were originally six independent claims. After the claim amendments and adding new claims described above, there are still 6 independent claims, but there are now 18 total claims. Since the number of independent claims has not changed and the number of total claims is less than or equal to 20, no additional fees are due. Therefore, Applicants submit claims 1-18 for further examination.

In the *Amendments to the Specification* section of this Amendment C, Applicants have amended the text on page 9 at line 20 of the original specification to remove the word "and" to correct a grammatical mistake and to clarify the sentence.

No new matter has been added by the above described amendments and new claims.

In the subject Office Action, the Examiner rejected claims 1-6 under 35 U.S.C. 112 second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. The Examiner specifically asserted that the list of potential operations for the multi-core/dual expander of claims 1-6 was indefinite because it was given as a list of potential example operations using the words "such as" instead of a specific operation or operations assigned as the various operations. As described above, Applicants have removed the list of potential operations from claims 1-6 and added Markush group dependent claims of the potential operations in claims 7-12. Therefore, claims 1-6 are not indefinite and claims 1-6 do not fail under 35 U.S.C. 112 second paragraph.

In the subject Office Action, the Examiner rejected claims 1 and 2 under 35 U.S.C. 102(b) as being anticipated by IEEE Standard Test Access Port and Boundary – Scan Architecture (hereinafter IEEE). The Examiner further rejected claims 1-6 under 35 U.S.C. 102(b) as being anticipated by Cyngal Application Note – Programming FLASH through the JTAG Interface (hereinafter Cyngal).

Turning first to IEEE, sections 5.1 and 5.2 on pages 17-18 of IEEE describe a system that requires an instruction register and at least one test data register as part of a group of test data registers. For instance, Figure 5-1 on page 18 of IEEE shows a separate "Instruction register" from "Test data registers." Further, section 5.1 on page 17 of IEEE states:

> "**5.1 Test logic design**
>
> **5.1.1 Specifications**
>
> **Rules**
>
> . . .
>
> b) The instruction and test data registers shall be separate shift-register based paths . . .
>
> c) The selection between the alternative instruction and test data register paths between TDI and TDO shall be made under the control of the TAP controller . . .
>
> **5.1.1 Description**
>
> . . .
>
> Key features of the design are as follows:
>
> . . .
>
> b) The instruction register. This allows the instruction to be shifted into the design. The instruction is used to select the test to be performed or the test data register to be accessed or both . . .
>
> c) The group of test data registers. The group of test data registers shall include a bypass and a boundary-scan register. It also may include an optional device identification register and further optional test data registers." *Emphasis added.*

Thus, the disclosure of IEEE describes a system with at least two shift registers, an "instruction register" and at least one "test data register."

Turning to Cyngal, there is similar disclosure of two registers, an "instruction register" (IR) and a "data register" (DR). As described in Figure 9 on page 8 of Cyngal, a read operation loads the instruction register (IR) with the register to be read and loads the data register (DR) with the 'Read' op code. As described in Figure 10 on page 9 of Cyngal, a write operation loads the instruction register (IR) with the register to be written and loads the data register (DR) with

the 'Write' op code and the data to be written. Figure 22 on page 18 of Cyngal also shows that all serially connected devices have both an "Instruction Register" and a "Data Register." Thus, like IEEE, Cyngal discloses a system that has two registers for handling communications, an "instruction register" and a "data register."

As amended claim 1 of the subject patent application recites: "using a test port of said multiple core expander to receive both data values as well as instructional and operational codes including a dummy bit from a host computer into a multi-bit shift register." *Emphasis added.* Thus, claim 1 recites a system that receives both data values and instructional/operational codes in a single multi-bit shift register. Both IEEE and Cyngal disclose systems that require a separate "instruction register" and a separate "data register." As such, both IEEE and Cyngal not only do not teach the single multi-bit shift register of the presently claimed invention, but in fact teach away from the use of a single multi-bit shift register by teaching the need for both an "instruction register" and a separate "data register."

It is axiomatic that the standard for lack of novelty under 35 U.S.C. 102 is one of strict identity. To anticipate a claim for a patent, a single prior source must contain all of the claim's essential elements. Both IEEE and Cyngal disclose systems that require at least two separate registers, an "instruction register" and a "data register." Claim 1 of the subject patent application discloses a single multi-bit shift register for sending and receiving data and instruction codes. Thus, neither IEEE nor Cyngal teach, disclose, or suggest the limitation for a single multi-bit shift register for sending/receiving both data and instructional codes. This function, taught and claimed by Applicants, is unique to Applicants. Therefore, neither IEEE nor Cyngal anticipate claims 1 of the subject patent application under 35 U.S.C. 102(b). Independent claims 2-6 of the subject patent application contain limitations similar to claim 1 and, therefore, are also not anticipated by IEEE or Cyngal under 35 U.S.C. 102(b) for the same reasons as described for claim 1. Claims 7-18 are dependent claims depending from independent claims 1-6. Since independent claims 1-6 are not anticipated by IEEE or Cyngal, dependent claims 7-18 are also not anticipated by IEEE or Cyngal under 35 U.S.C. 102(b).

For the reasons stated above, claims 1-18 are considered to be patentable over the prior art. Therefore, this application is now considered to be in condition for allowance and such action is earnestly solicited.

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